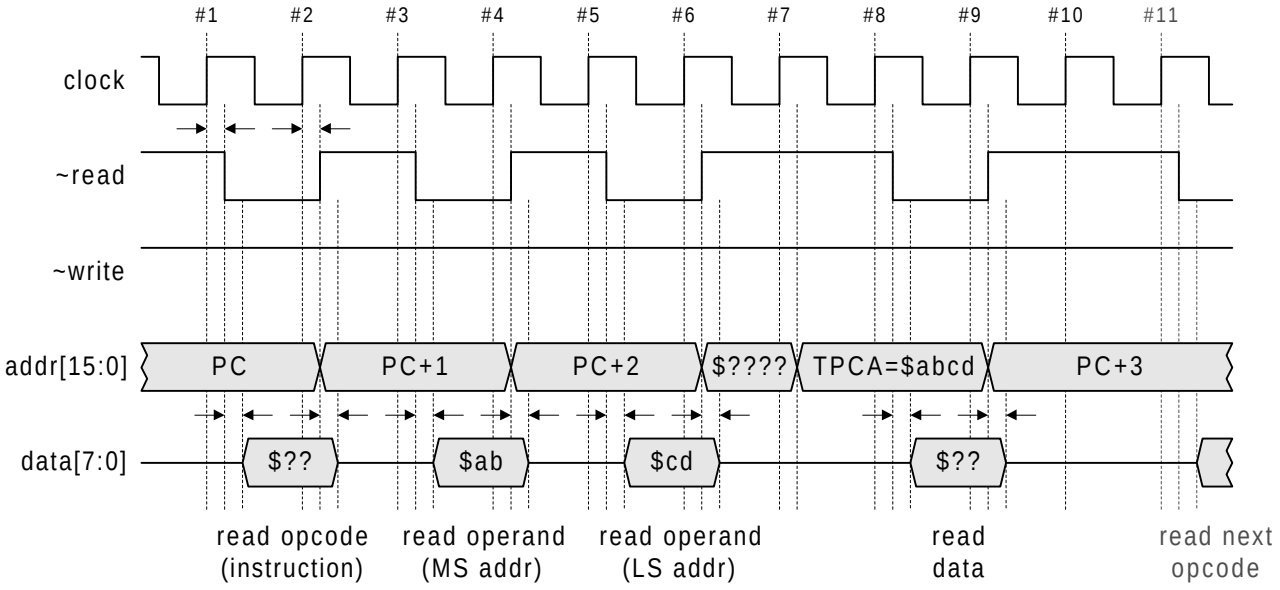
PhizzyB Clock Cycles versus Instructions

On the following pages you will find tables showing the number of clock cycles required to execute each *Beboputer/PhizzyB* instruction for every addressing mode.

These tables are extracted from Appendix C of *The Official Beboputer Microprocessor Databook*, which is available as a machine-readable E-book (electronic book) for only $14.95 US Dollars, and which can be downloaded from the Maxfield & Montrose Web site at **www.maxmon.com**

For each instruction type and addressing mode combination, Appendix C provides a timing diagram as shown below, followed by a detailed clock-by-clock analysis of what's happening inside the CPU.

This information is of interest to anyone who wants to gain a deeper insight as to how each instruction type is executed, and the overhead associated with each instruction/mode in terms of CPU clock cycles.



Example figure from Appendix C of
The Official Beboputer Microprocessor Databook

	imp		imm		abs		abs-x		ind		x-ind		ind-x	
	op	#	op	#	op	#	op	#	op	#	op	#	op	#
ADD			$10	5	$11	10	$12	10						
ADDC			$18	5	$19	10	$1A	10						
AND			$30	5	$31	10	$32	10						
BLDIV			$F0	7	$F1	11								
BLDSP			$50	7	$51	11								
BLDX			$A0	7	$A1	11								
BSTSP					$59	13								
BSTX					$A9	13								
CLRIM	$09	3												
CMPA			$60	5	$61	10	$62	10						
DECA	$81	3												
DECX	$83	3												
HALT	$01	3												
INCA	$80	3												
INCX	$82	3												
JC					$E1	*7								
JMP					$C1	7	$C2	8	$C3	12	$C4	12	$C5	13
JN					$D9	*7								
JNC					$E6	*7								
JNN					$DE	*7								
JNO					$EE	*7								
JNZ					$D6	*7								

* The conditional jump instructions (JC, JNC, JN, JNN, ...) require 7 clock cycles if the test passes, but only 4 clock cycles if the test fails.

Legend

op = Opcode
$ = Hexadecimal number
# = Number of clocks to execute this instruction

Addressing Modes

imp = Implied
imm = Immediate
abs = Absolute
abs-x = Indexed
ind = Indirect
x_ind = Pre-indexed indirect
ind-x = Indirect post-indexed

	imp		imm		abs		abs-x		ind		x-ind		ind-x	
	op	#	op	#	op	#	op	#	op	#	op	#	op	#
JO					$E9	*7								
JSR					$C9	13	$CA	14	$CB	18	$CC	18	$CD	19
JZ					$D1	*7								
LDA			$90	4	$91	9	$92	9	$93	14	$94	14	$95	14
NOP	$00	3												
OR			$38	5	$39	10	$3A	10						
POPA	$B0	5												
POPSR	$B1	5												
PUSHA	$B2	6												
PUSHSR	$B3	6												
ROLC	$78	3												
RORC	$79	3												
RTI	$C7	10												
RTS	$CF	8												
SETIM	$08	3												
SHL	$70	3												
SHR	$71	3												
STA					$99	10	$9A	10	$9B	15	$9C	15	$9D	15
SUB			$20	5	$21	10	$22	10						
SUBC			$28	5	$29	10	$2A	10						
XOR			$40	5	$41	10	$42	10						

* The conditional jump instructions (JC, JNC, JN, JNN, ...) require 7 clock cycles if the test passes, but only 4 clock cycles if the test fails.

Legend

op = Opcode
$ = Hexadecimal number
# = Number of clocks to execute this instruction

Addressing Modes

imp = Implied
imm = Immediate
abs = Absolute
abs-x = Indexed
ind = Indirect
x_ind = Pre-indexed indirect
ind-x = Indirect post-indexed